Implementation of Vedic Multiplier on Circuit Level

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Abstract—*Multipliers are the basic building blocks of any ALU thus speed of ALU depends upon multiplier. Vedic Mathematics is used for fastest calculation, using same concept 8x8 multiplier is implemented on circuit level and simulated on Tanner tool. There are 16 Sutra and 13 sub Sutra in Vedic Mathematics. One of the 16 Sutra is Urdhva Tiryagbhyam which is the most efficient for arithmetic multiplication resulting minimum delays.*

Keywords— ALU, Atharva Veda, Urdhva Tiryagbhyam, Vedic Mathematics, Vedic Multiplier*.*

I. INTRODUCTION

Vedic Mathematics: The ancient sages of India have given a wonderful gift to the world "*Vedic Mathematic"*. *By* using Vedic Mathematics one can solve the tedious calculations into simpler, orally manageable operation without pen and paper. It is introduced by Swami Bharati Krishna Tirtha (1884-1960), former Jagadguru Sankaracharya of Puri culled a set of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the Atharva Veda [1].

Earlier only array multiplier is used .In 2 bit binary array multiplication the product is obtain by calculating partial products firstly then these partial products are summed together thus requiring more number of gates resulting more delay and hence less economic. Efficiency of array multiplier can be improved by using CSA and Wallace Tree method. The limitation of CSA method is in its execution time, which depends upon the number of bits of the multiplier; due to this there is some difficulty in achieving high speed operation [3]. In the Wallace tree method, the circuit layout is not easy although the speed of the operation is high since the circuit is quite irregular. So a new multiplier is designed using Vedic mathematics Known as Vedic multiplier, which is faster than other existing multipliers.

In this paper, implementation of 8x8 Vedic multiplier on circuit level is done by using the sutra of Vedic Mathematics called Urdhva Tiryagbhyam, on Tanner Tool and power dissipation and time delay is calculated.

1.1 Vedic Formulae

The word 'Vedic' is derived from the word 'Veda' which means the unlimited knowledge. Vedic mathematics is mainly based on 16 Sutras dealing with various branches of mathematics like arithmetic, algebra, geometry etc. In this paper we discuss only one of them i.e. Urdhav-Tiryagbhyam.

1.1.1Urdhav-Tiryagbhyam

It means "vertical and crosswise".Example for 2 bit multiplication is shown below:

(1) 23 X 44

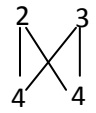

Fig.1 Multiplication of 2 bit

Step 1. 3x4=12
Step 2 . 2x4+3x4= 20
Step 3 2x4=8

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  8 0 2
+ 2 1
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10 12
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Thus 23 x 44=1012

Similarly for 4 bit multiplication will be done.

(2) 123 X 143

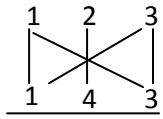

Fig.2 Multiplication of 3 bit

Step 1. 3*3= 9
Step 2 . 2*3+3*4= 18
Step 3 1*3+2*4+1*3=14
Step 4. 1*4 +2*1 = 6
Step5 . 1*1=1

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  1648 9
+   1 1
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 17589
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Thus 123 x143=17589

II. DESIGN OF VEDIC MULTIPLIER

Design is implemented on Tanner Tool, means on circuit level. 8 x 8 Vedic Multiplier is implemented in same fashion as 2x2 Vedic Multiplier. Circuit diagram of 2x2 Vedic Multiplier is shown below:

A1 A0
B1 B0
P3 P2 P1 P0

Final product can be represented as follows:

P0 = A0*B0

P1 = A1*B0+A0*B1+Carry

P2 = A1*B1+ Previous Carry from P1

P3 = carry generated by P2

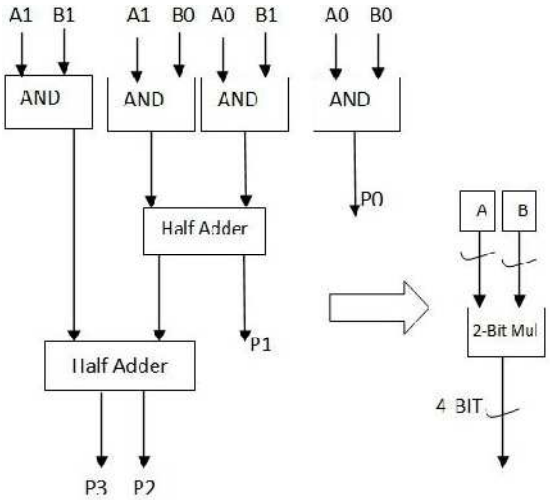

Fig. 3- 2Bit multiplier using Urdhva Tiryakbhyam Sutra & its symbol

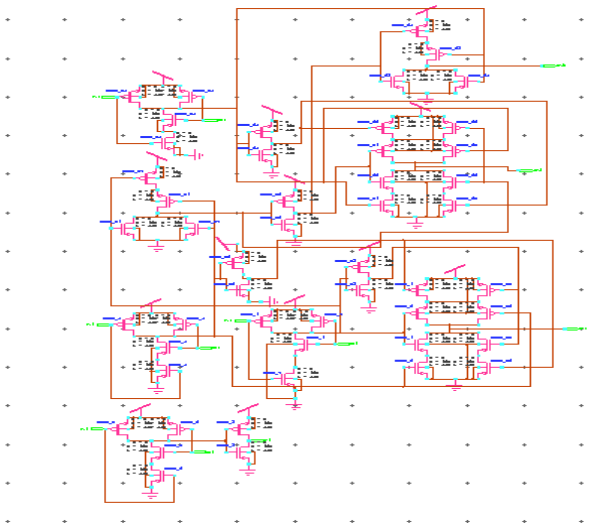

Fig. 4-Schmetic of 2Bit multiplier using Urdhva Tiryakbhyam Sutra

Similarly 4x4 Vedic multiplier and 8x8 Vedic multiplier is implemented and analyzed .4x4 Vedic Multiplier Hardware architecture is given below:

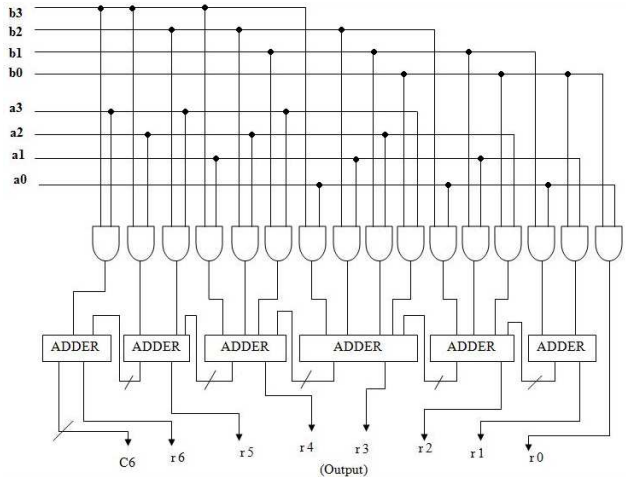

Fig. 5- Hardware architecture of4Bit multiplier using Urdhva Tiryakbhyam Sutra

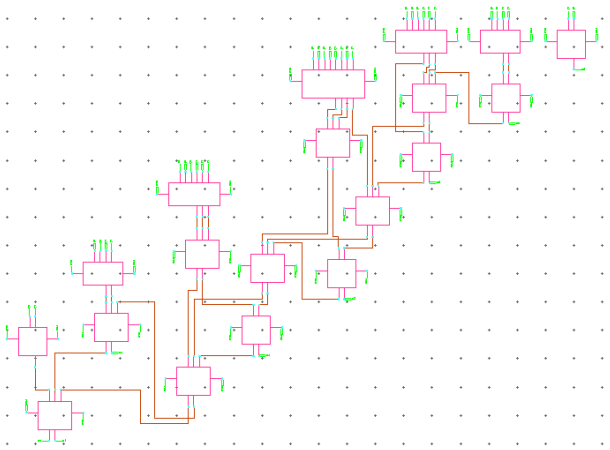

Fig. 6-Schmetic of 4Bit multiplier using Urdhva Tiryakbhyam Sutra

III. RESULT

The simulation result obtain is summarized in table.1 which represent average power consumption and delay time which is shown below.

Table 1.Power consumption and Delay time of different multiplier.

Type of multiplier	Average Power(Watt)	Delay Time (ns)
2 bit	$8.88X10^{-5}$	$4.3X10^{-11}$
4 bit	$1.11X10^{-5}$	$9.2X10^{-11}$
8 bit	$1.46X10^{-4}$	$1.9X10^{-8}$

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Above Table shows result of different bit size multiplier.

IV. CONCLUSION

This paper shows an efficient binary Vedic multiplier design in circuit level. By using above mentioned multiplier we get almost 70% power reduction as compared with other convention multiplier on gate level. This design reduces calculation steps resulting in high speed. As they

give high speed, hence suitable for DSP processor and VLSI processor.

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